DFEA2 testing

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2. Bit to bit comparison using test vector
3. DFEA2 Data base interface
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Status of DFEA2 test at FNAL

Currently we have three types of setup for DFEA2 board test at FermiLab.

* DFEA2 Stand Alone Test (DSAT)
* DFEA2 Test stand
* D0 Platform Test

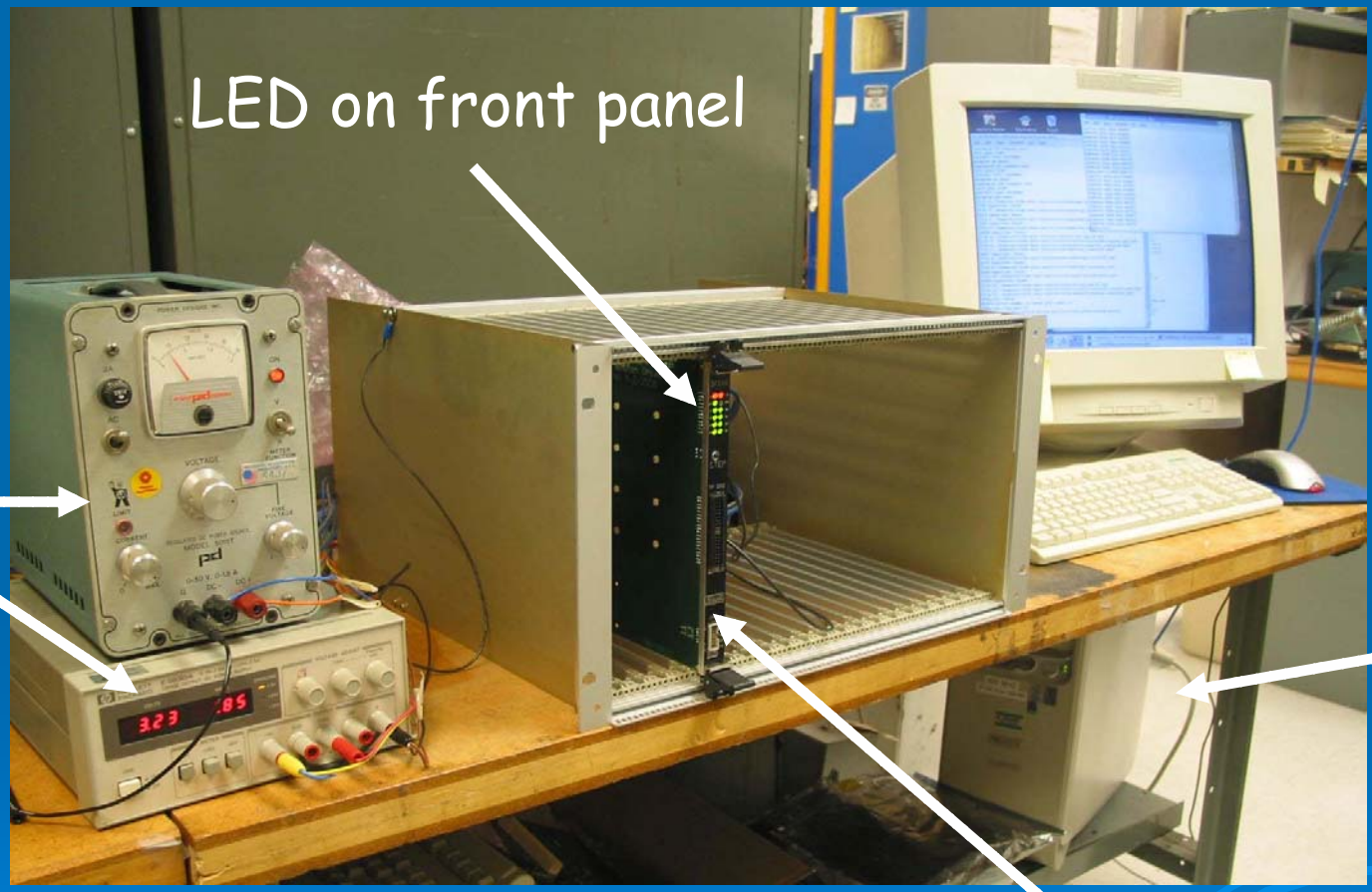
DSAT setup

The setup consists of :

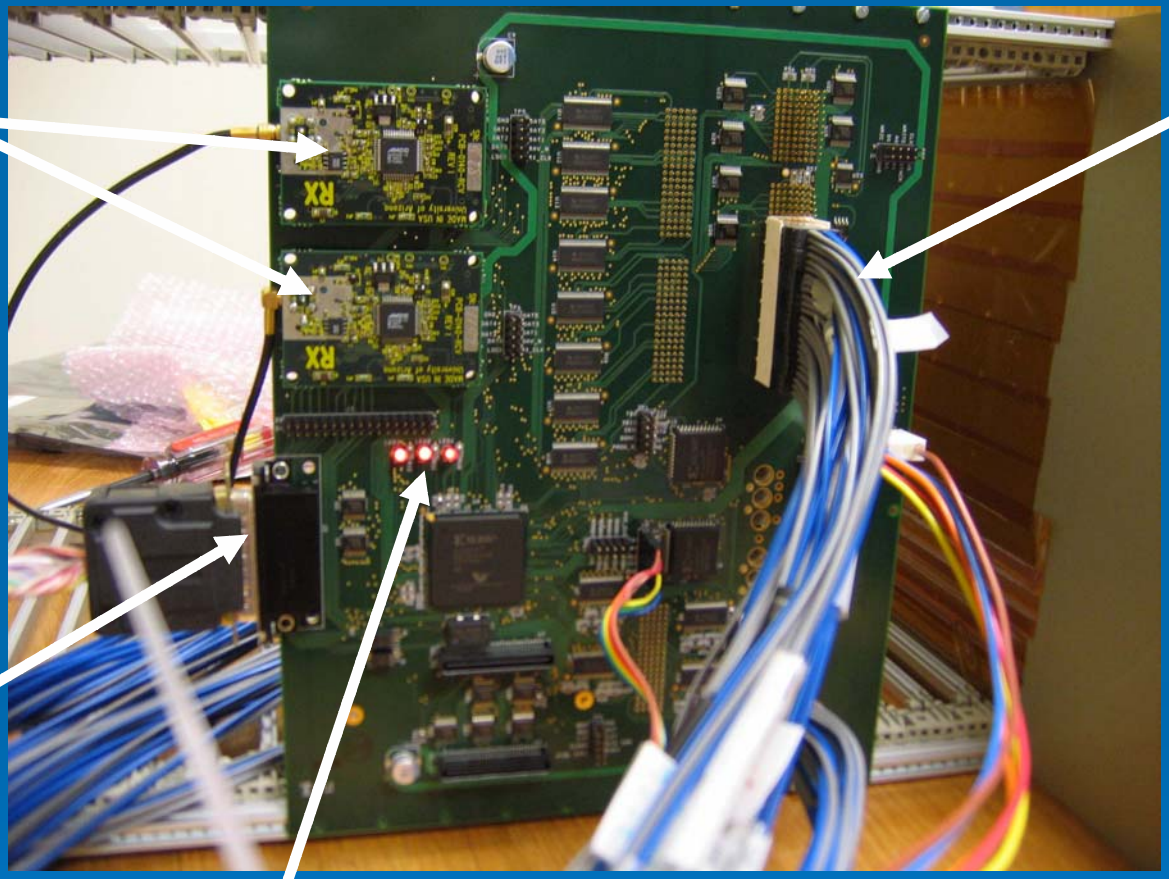
* Linux PC, connected to DSAT through the Parallel Port.
* DSAT board, connected to single DFEA2 board through the LVDS cables.
* Power supplies for DSAT board and DFEA2 single board (3.3V, 5V, and 48V).
* DFEA2 crate

DSAT setup

From the beginning of June 2005 the copy of DSAT was setting up at Fermilab and located on DAB3.



DSAT backplane



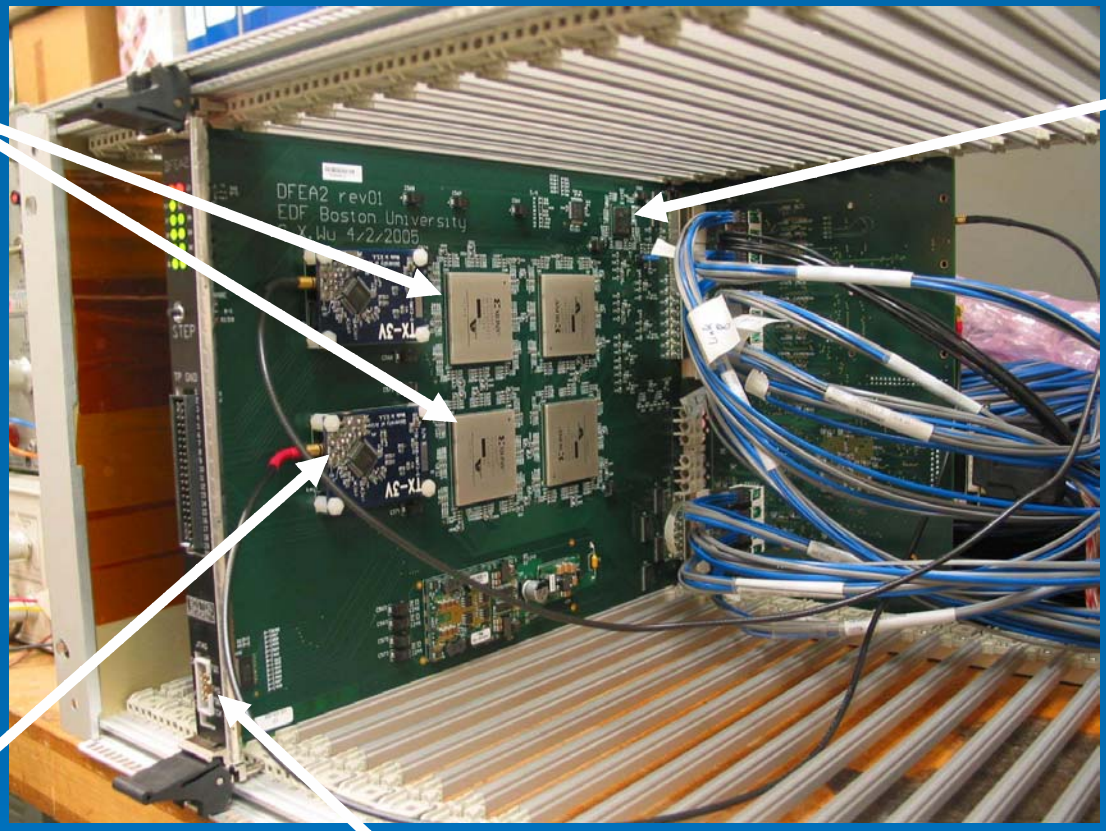
DSAT and DFEA2 board

Top and bottom firmwares:

(U7, U8, U9, U10)

Xilinx chips:

XC2V6000



U6 firmware

Mounted new transmitters

JTAG input. New version of u6vc.mcs downloaded (U6 firmware) on all the boards.

Results of the link test

Random link test was done at Fermilab for 49 boards. Number of cycling 2000. Each cycling generates 73 random events. About 2.5 hours/board.

* 46 boards passed the test with zero errors.
  - 1 board had powered problem.
  - 2 boards initialization problem.

  } sent back to BU.

* Of 46 boards 33 have new transmitters mounted on them. The boards passed the test again after the transmitters were mounted.

* New U6 firmware downloaded on all boards

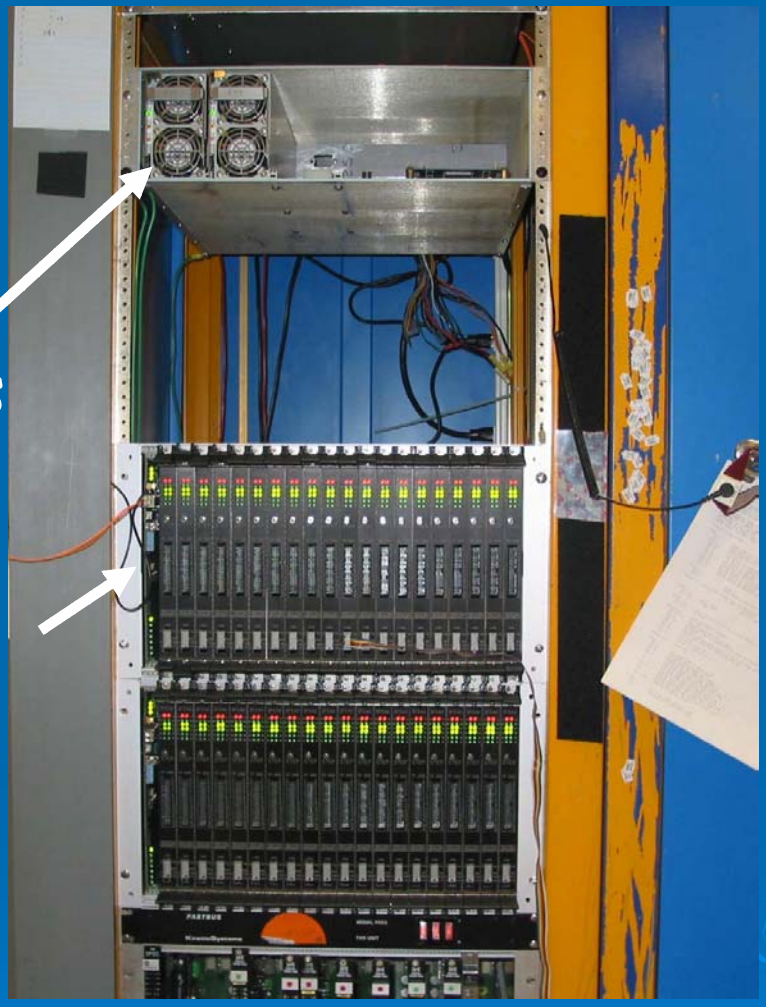
Test stand

The test stand functionality:

Load vector into the input buffers, send them through the design and capture the output.

2 power supplies

DFEC2 controller



Powered-on 40 boards on test stand in 2 crates.

Bit to bit comparison using the Test Vector

5000 real events were used (Dumpster program, on d0ol10) from platform for detail bit to bit comparison.

Number of events is limited only due to big size of output text file. 1Kevent -> 1.6MB

Incapture program (Jamieson-linux PC) reads the output file of Dumpster in ASCII format, extracts the 8 links input test vector from the file and use as an Input vector for DFEA2 on test stand.

Comparison using the test vector

The Comp2fileTestVector code was developed for bit to bit comparison of two files containing DFEA2 output buffer information.

Input files can be real data or simulated data.

In this analysis I used the real data from the platform and test stand.

Comparison using the test vector

What does the Comp2fileTestVector? (I)

```
*** DFEA2 event dump 1 of 1000 ***

Status registers:
R00: 0001       R01: 0043       R02: 0000       R03: 27FF       R04: 0007
R05: 0007
R06: 0007       R07: 0007       R08: 0E33       R09: 0000       R10: FF00
R11: 2121
top sector = 0  bot sector = 1

Inputs:
link1:  0180000 0100000 0000080 0004010 0800000 0800000 0080041
link2:  0002080 0000080 0000000 0000000 0000000 0000010 0000201
link3:  8004200 8000004 0020020 4020000 0008080 0008000 040A111
link4:  0800040 4000000 0800002 0800000 0880020 0000020 0404001
link5:  0000110 0000008 0000020 0000120 0000080 2000008 2000011
link6:  0001000 0011000 0010010 0051800 0060000 0000800 0020001
link7:  0400000 0400000 0420800 0020000 0020840 0000800 0000001
link8:  4102000 1000000 0008000 0008000 0002000 8022000 0080003

L1 output to CTOC:
top:    E00002F 0000000 0000000 0000000 0000000 0001600 0000000
bot:    E00012F 0000000 0000000 0000000 0000000 0001900 0000000

L2CFT output to CTOC:
top:    E000028 0031986 0000000 0000000 0000000 0000000 0000000 0000000 0000000
0000000 0000000 0000000 0000000 0000000 0000000 0000000 0000000 0000000 0000000
0000000 0000000 0000000 0000000 0000000 0000000 0000000 0000000
bot:    E000028 0031986 0010000 0010000 0010000 0010000 0010000 0010000 0010000
0010000 0010000 0010000 0010000 0010000 0010000 0010000 0010000 0010000 0010000
0010000 0010000 0010000 0010000 0010000 0010000 0010000 0000000

L2CPS output to CTOC:
top:    E0000C0 0031986 0000000 0000000 0000000 0000000 0000000 0000000 0000000
0000000 0000000
bot:    E0000C0 0031986 0000000 0000000 0000000 0000000 0000000 0000000 0000000
0000000 0000000

L1 output to muon:
top:    0000    0000    0000    0000    0000    0000    0000
bot:    0000    0000    0000    0000    0000    0000    0000
```

Dumpster output format

- read the information of input files, identify the corresponding event number from both files
- make the loop inside the event
- identify the information:
  - L1 output to CTOC
  - L2 CPS output to CTOC
  - L1 output to Muon

Comparison using the test vector

What does the Comp2fileTestVector? (II)

```
*** DFEA2 event dump 1 of 1000 ***

Status registers:
R00: 0001       R01: 0043       R02: 0000       R03: 27FF       R04: 0007
R05: 0007
R06: 0007       R07: 0007       R08: 0E33       R09: 0000       R10: FF00
R11: 2121
top sector = 0  bot sector = 1

Inputs:
link1:  0180000 0100000 0000080 0004010 0800000 0800000 0080041
link2:  0002080 0000080 0000000 0000000 0000000 0000010 0000201
link3:  8004200 8000004 0020020 4020000 0008080 0008000 040A111
link4:  0800040 4000000 0800002 0800000 0880020 0000020 0404001
link5:  0000110 0000008 0000020 0000120 0000080 2000008 2000011
link6:  0001000 0011000 0010010 0051800 0060000 0000800 0020001
link7:  0400000 0400000 0420800 0020000 0020840 0000800 0000001
link8:  4102000 1000000 0008000 0008000 0002000 8022000 0080003

L1 output to CTOC:
top:    E00002F 0000000 0000000 0000000 0000000 0001600 0000000
bot:    E00012F 0000000 0000000 0000000 0000000 0001900 0000000

L2CFT output to CTOC:
top:    E000028 0031986 0000000 0000000 0000000 0000000 0000000 0000000
0000000 0000000 0000000 0000000 0000000 0000000 0000000 0000000 0000000
0000000 0000000 0000000 0000000 0000000 0000000 0000000 0000000 0000000
bot:    E000028 0031986 0010000 0010000 0010000 0010000 0010000 0010000 0010000
0010000 0010000 0010000 0010000 0010000 0010000 0010000 0010000 0010000
0010000 0010000 0010000 0010000 0010000 0010000 0010000 0000000

L2CPS output to CTOC:
top:    E0000C0 0031986 0000000 0000000 0000000 0000000 0000000 0000000 0000000
0000000 0000000
bot:    E0000C0 0031986 0000000 0000000 0000000 0000000 0000000 0000000 0000000
0000000 0000000

L1 output to muon:
top:    0000    0000    0000    0000    0000    0000    0000
bot:    0000    0000    0000    0000    0000    0000    0000
```

7 TSL

27

11

7

- make the loop by time slices for each output and compare bit to bit.
- if there is a difference then unpack the information according to the Data transfer protocols.

1.1 DFEA to CTOC

Frame	BoR			HP	Third Byte								Second Byte								First Byte							
	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
F1/HF	1	1	1	HP	P/M			OCT			CR	FX	0	0	0	0	RA TS CFT/CPSax				L1CTT/PS DATA TYPE					L1/L2		
F2	0	0	0	HP	XPT+LC			XPT-LC			0	0	XPT+TC			XPT-TC			0	0	XPT+NC			XPT-NC			0	0
F3	0	0	0	HP	HPT+LC			HPT-LC			0	0	HPT+TC			HPT-TC			0	0	HPT+NC			HPT-NC			0	0
F4	0	0	0	HP	MPT+LC			MPT-LC			0	0	MPT+TC			MPT-TC			0	0	MPT+NC			MPT-NC			#PSC	
F5	0	0	0	HP	LPT+LC			LPT-LC			0	0	LPT+TC			LPT-TC			0	0	LPT+NC			LPT-NC			0	0
F6	0	0	0	HP	SUM ABS[PT]						0	0	OL TS								ISOLATED TRACK TS							
F7/TF	0	0	0	0	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP

Comparison using the test vector

What does the Comp2fileTestVector? (III)

- report differences: event number, L1/2 output, bot or top sector, time slice and unpack data for both files.

- finally count errors for unpacked data and make summary table.

DFEA2 I/O buffer information

Example

Platform (Dumpster)

```
*** DFEA2 event dump 1 of 1000 ***

Status registers:
R00: 0001       R01: 0043       R02: 0000       R03: 27FF       R04: 0007
R05: 0007
R06: 0007       R07: 0007       R08: 0E33       R09: 0000       R10: FF00
R11: 2121
top sector = 0  bot sector = 1

Inputs:
link1:  0180000 0100000 0000080 0004010 0800000 0800000 0080041
link2:  0002080 0000080 0000000 0000000 0000000 0000010 0000201
link3:  8004200 8000004 0020020 4020000 0008080 0008000 040A111
link4:  0800040 4000000 0800002 0800000 0880020 0000020 0404001
link5:  0000110 0000008 0000020 0000120 0000080 2000008 2000011
link6:  0001000 0011000 0010010 0051800 0060000 0000800 0020001
link7:  0400000 0400000 0420800 0020000 0020840 0000800 0000001
link8:  4102000 1000000 0008000 0008000 0002000 8022000 0080003

L1 output to CTOC:
top:    E00002F 0000000 0000000 0000000 0000000 0001600 0000000
bot:    E00012F 0000000 0000000 0000000 0000000 0001900 0000000

L2CFT output to CTOC:
top:    E000028 0031986 0000000 0000000 0000000 0000000 0000000 0000000 0000000
0000000 0000000 0000000 0000000 0000000 0000000 0000000 0000000 0000000 0000000
0000000 0000000 0000000 0000000 0000000 0000000 0000000 0000000
bot:    E000028 0031986 0010000 0010000 0010000 0010000 0010000 0010000 0010000
0010000 0010000 0010000 0010000 0010000 0010000 0010000 0010000 0010000 0010000
0010000 0010000 0010000 0010000 0010000 0010000 0010000 0000000

L2CPS output to CTOC:
top:    E0000C0 0031986 0000000 0000000 0000000 0000000 0000000 0000000 0000000
0000000 0000000
bot:    E0000C0 0031986 0000000 0000000 0000000 0000000 0000000 0000000 0000000
0000000 0000000

L1 output to muon:
top:    0000    0000    0000    0000    0000    0000    0000
bot:    0000    0000    0000    0000    0000    0000    0000
```

Test stand (Incapture)

```
*** DFEA2 event 1 ***

Status registers:
R00: EE01       R01: 0043       R02: 0000       R03: 36FF       R04: 0007
R05: 0007
R06: 0007       R07: 0007       R08: 0E00       R09: FFFF       R10: FFFF
R11: 2121
top sector = 0  bot sector = 1

Inputs:
link1:  0180000 0100000 0000080 0004010 0800000 0800000 0080041
link2:  0002080 0000080 0000000 0000000 0000000 0000010 0000201
link3:  8004200 8000004 0020020 4020000 0008080 0008000 040A111
link4:  0800040 4000000 0800002 0800000 0880020 0000020 0404001
link5:  0000110 0000008 0000020 0000120 0000080 2000008 2000011
link6:  0001000 0011000 0010010 0051800 0060000 0000800 0020001
link7:  0400000 0400000 0420800 0020000 0020840 0000800 0000001
link8:  4102000 1000000 0008000 0008000 0002000 8022000 0080003

L1 output to CTOC:
top:    E00002F 0000000 0000000 0000000 0000000 0001600 0000000
bot:    E00012F 0000000 0000000 0000000 0000000 0001900 0000000

L2CFT output to CTOC:
top:    E000028 0000000 0000000 0000000 0000000 0000000 0000000 0000000 0000000
0000000 0000000 0000000 0000000 0000000 0000000 0000000 0000000 0000000 0000000
0000000 0000000 0000000 0000000 0000000 0000000 0000000 0000000
bot:    E000028 0000000 0010000 0010000 0010000 0010000 0010000 0010000 0010000
0010000 0010000 0010000 0010000 0010000 0010000 0010000 0010000 0010000 0010000
0010000 0010000 0010000 0010000 0010000 0010000 0010000 0000000

L2CPS output to CTOC:
top:    E0000C0 0000000 0000000 0000000 0000000 0000000 0000000 0000000 0000000
0000000 0000000
bot:    E0000C0 0000000 0000000 0000000 0000000 0000000 0000000 0000000 0000000
0000000 0000000

L1 output to muon:
top:    0000    0000    0000    0000    0000    0000    0000
bot:    0000    0000    0000    0000    0000    0000    0000
```

8 links input information from Platform data was used as an input test vector to Test stand.

Results of comparison

Several corrections were done in analysis mainly due to the absence of corresponding data on test stand, in particular:

- turn number (for CFT and CPS)
- crossing number (for CFT and CPS)
- Relative address of a trigger sector within the octant (TSL-1, bits: 08-11)
- Isolated track in trigger sector (TSL-6, CTOC)

...

Main corrections (for CFT/CPSax)

1.1 DFEA to CTOC

Frame	BoR			HP	Third Byte								Second Byte								First Byte							
	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
F1/HF	1	1	1	HP	P/M		OCT			CR	FX	0	0	0	0	RA TS CFT/CPSax					L1CTT/PS DATA TYPE					L1/L2		
F2	0	0	0	HP	XPT+LC			XPT-LC			0	0	XPT+TC			XPT-TC			0	0	XPT+NC			XPT-NC			0	0
F3	0	0	0	HP	HPT+LC			HPT-LC			0	0	HPT+TC			HPT-TC			0	0	HPT+NC			HPT-NC			0	0
F4	0	0	0	HP	MPT+LC			MPT-LC			0	0	MPT+TC			MPT-TC			0	0	MPT+NC			MPT-NC			#PSC	
F5	0	0	0	HP	LPT+LC			LPT-LC			0	0	LPT+TC			LPT-TC			0	0	LPT+NC			LPT-NC			0	0
F6	0	0	0	HP	SUM ABS[PT]						0	0	OL TS								ISOLATED TRACK TS							
F7/TF	0	0	0	0	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP

2.1 DFEA to CTOC, L2CFT Data (*identical to DFEA to STOV/STSX*)

Frame	BoR			HP	Third Byte								Second Byte								First Byte							
	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
F1/HF	1	1	1	HP	P/M		OCT			#OBJ VP			#OBJ MSB			#OBJ LSB			#OBJ HP		L1CTT/PS DATA TYPE					L1/L2		
F2/HF	0	0	0	HP	TURN NUMBER																CROSSING NUMBER							
F3/D1	0	0	0	HP	RA PSC CPSax			RA TS CFT/CPSax					T	L	C	PT BIN			PT EXT		R	RA CFT H-DOUBLET						ISO	
...	0	0	0	HP	.....																							
Fn/TF	0	0	0	0	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP

2.2 DFEA to CTOC, L2CPSax Data

Frame	BoR			HP	Third Byte								Second Byte								First Byte							
	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
F1/HF	1	1	1	HP	P/M		OCT			#OBJ VP			#OBJ MSB			#OBJ LSB			#OBJ HP		L1CTT/PS DATA TYPE					L1/L2		
F2/HF	0	0	0	HP	TURN NUMBER																CROSSING NUMBER							
F3/D1	0	0	0	HP	0	RA PSC CPSax			PSC WIDTH				T	L	C	PT BIN			PT EXT		R	RA TS CFT/CPSax			0	0		ISO
...	0	0	0	HP	.....																							
Fn/TF	0	0	0	0	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP	VP

- main corrections

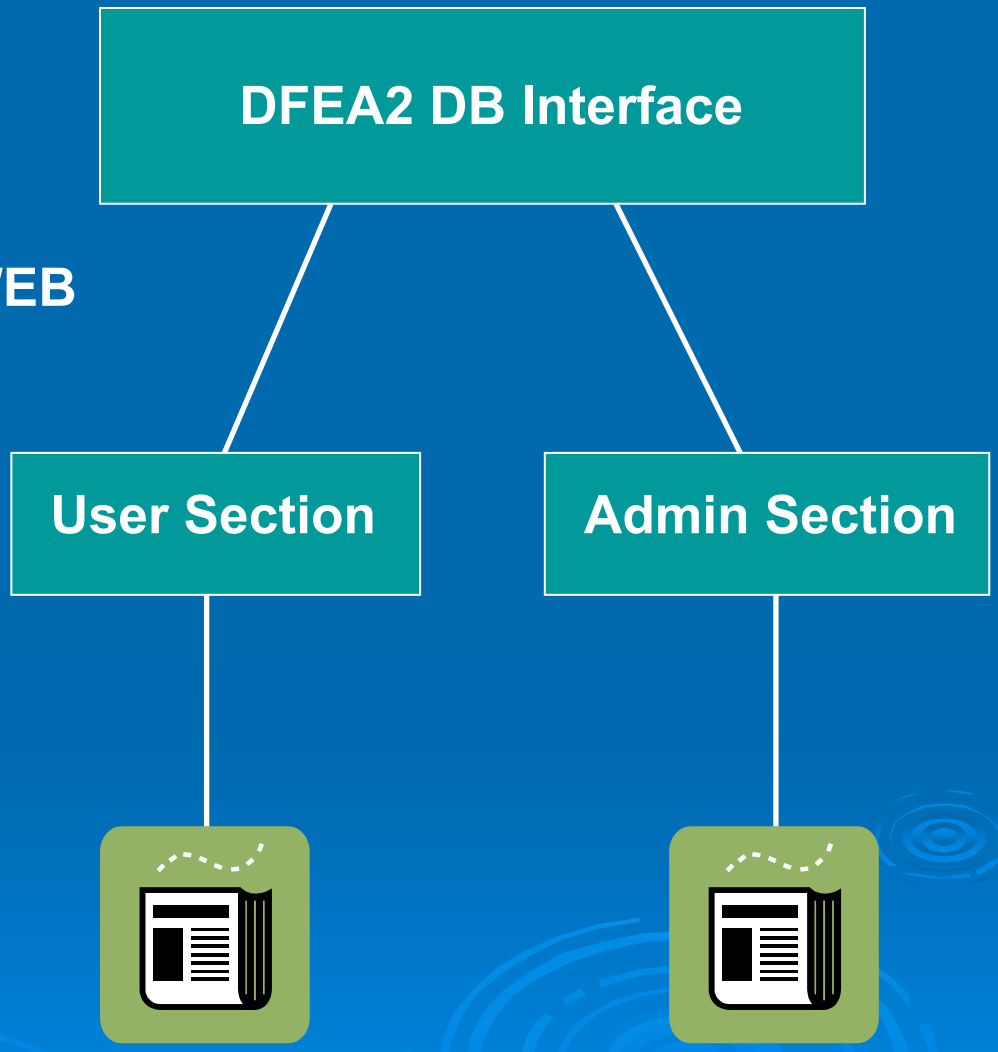
Results of comparison

After the all corrections the data from platform and test vector on test stand are in good agreement.

DFEA2 Data Base Interface

Outline

- Store DFEA2 information in Data Base
- Ability to access these data through WEB
- Facility to add/change/remove it

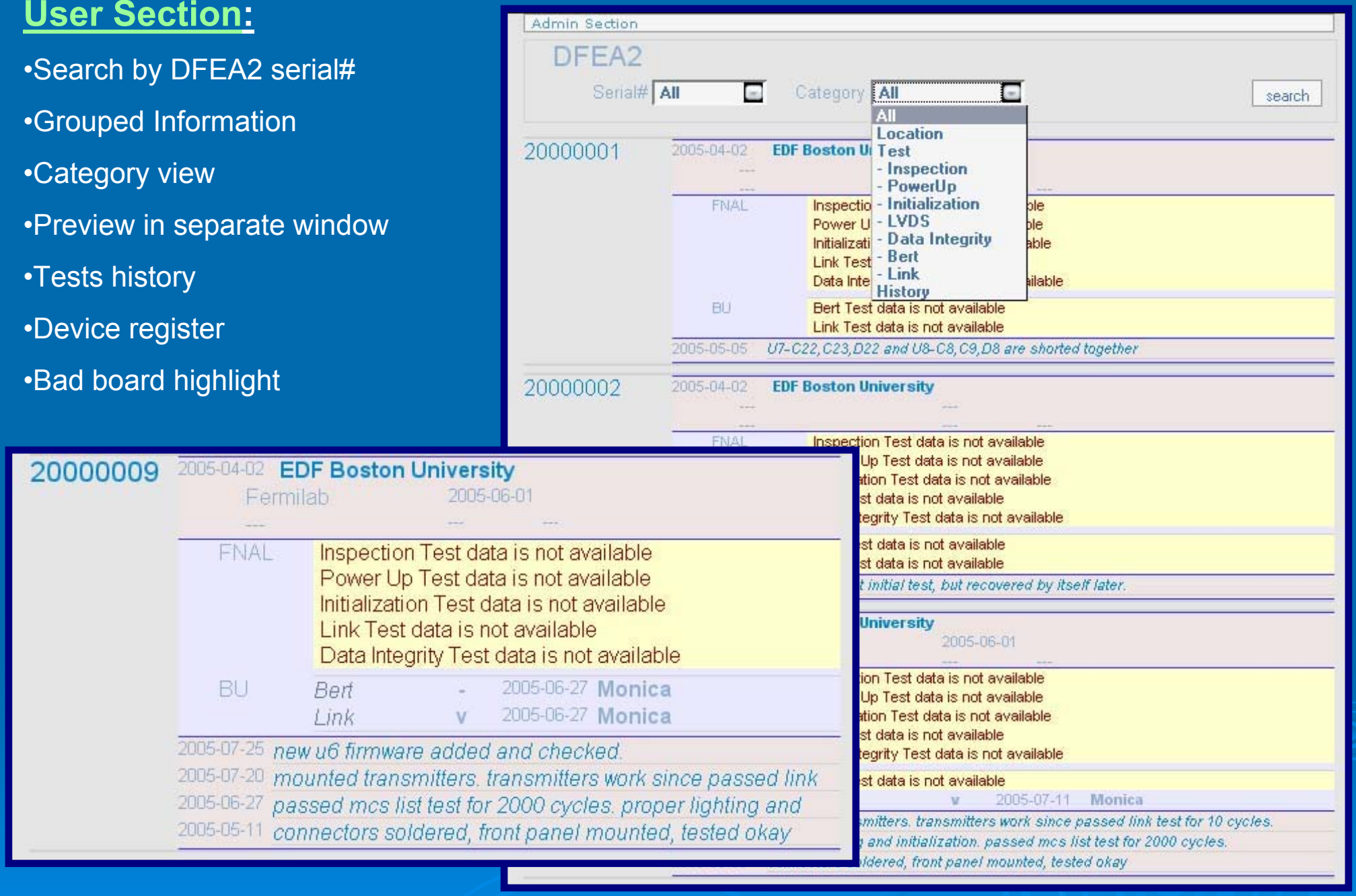


Resulting Interface can be found at:

http://dzero.bu.edu/~d0ctt/

User Section:

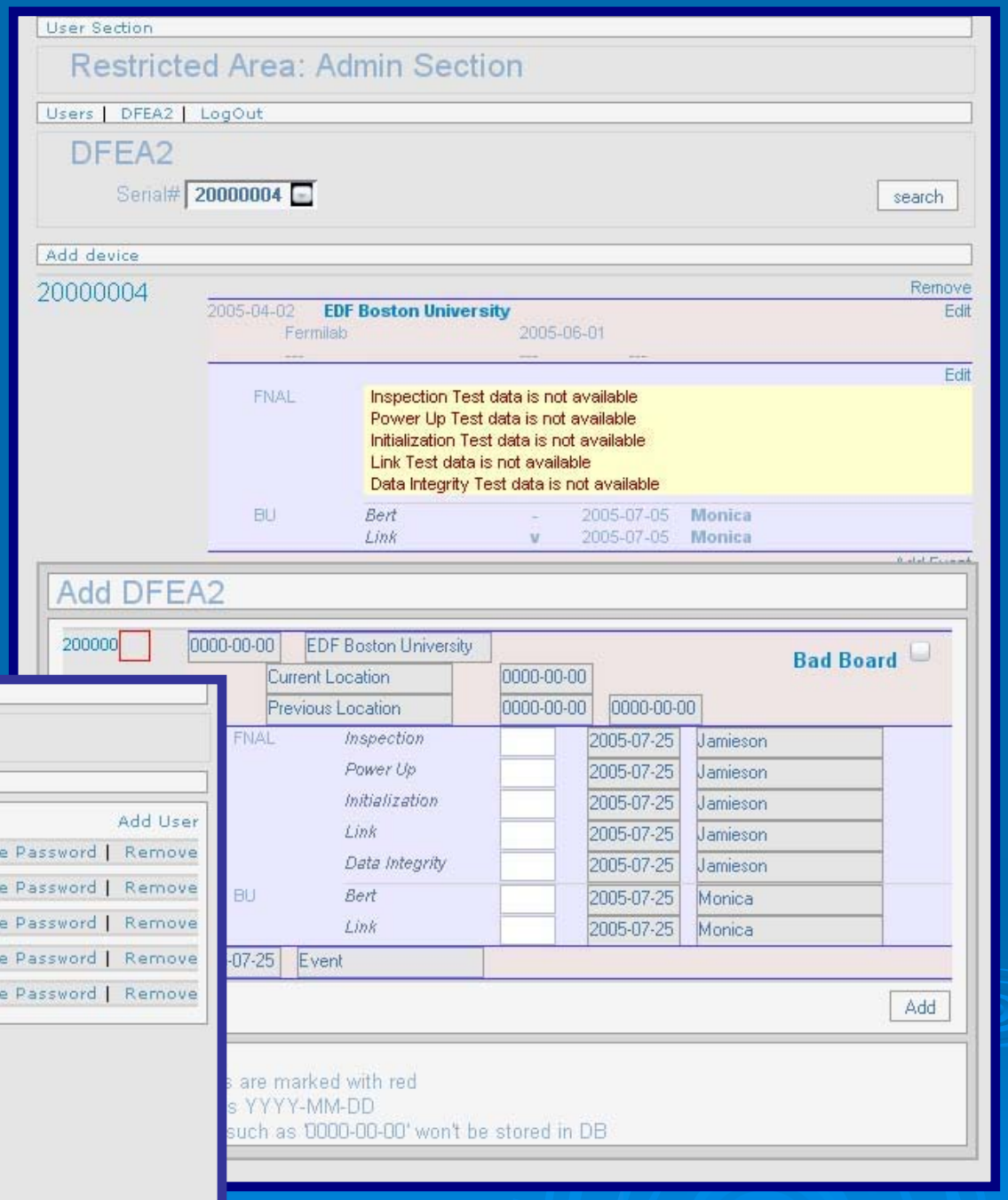
- Search by DFEA2 serial#
- Grouped Information
- Category view
- Preview in separate window
- Tests history
- Device register
- Bad board highlight

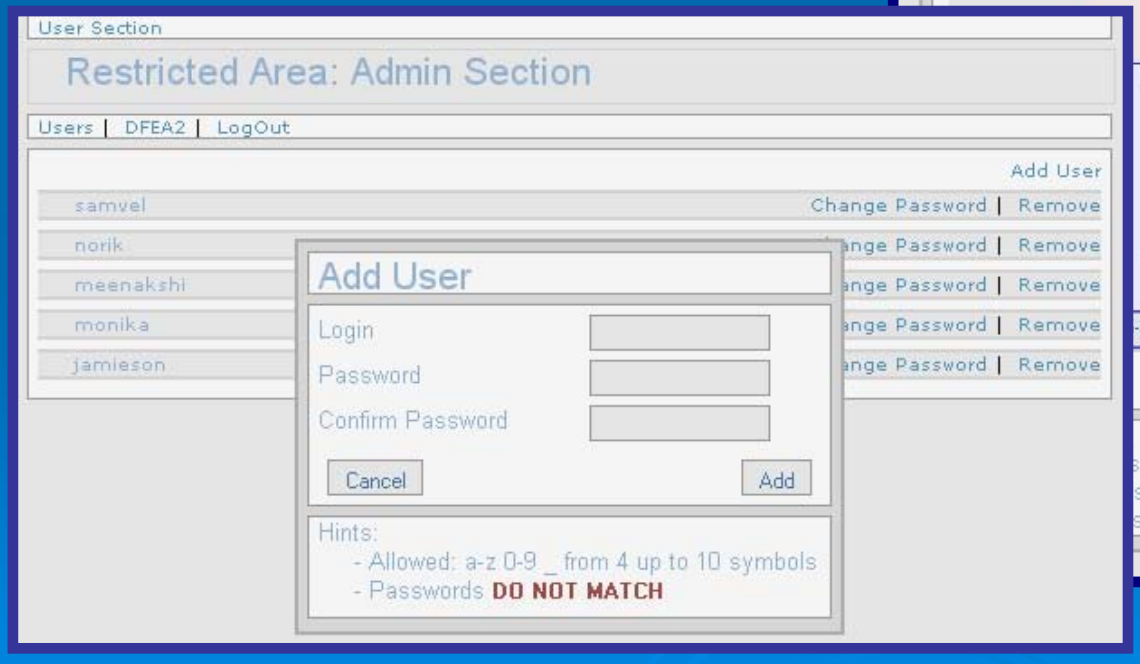


(Prepared by Samvel Khalatian)

Admin Section:

- Security
- DFEA2 management interface:
  - Add/Remove
  - Modify existing information
  - Add notes
- Users management:
  - Add/Remove
  - Edit user profile





(Prepared by Samvel Khalatian)

DFEA2 Firmware Generation

Test Generation of DFEA2 firmware were performed on cartman-clued0.fnal.gov which is dual Intel® Xeon™ CPU 2.4 GHz processor machine

Preliminary Results

# of Chips	# of Sectors	Time taken (hours)
1	½	2
2	1	4
4	2	8

320 CPU hours are needed to generate all 80 sectors (2 chips per sector)